Original Research Article

Conventional silicate scaling structure for gate dielectric material

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Abstract The scaling of device structure compels look for a replacement of conventional SiO_2, used as gate dielectric material for last 5 decades, by high-dielectric materials. The IL results in lowering of overall dielectric constant of the gate dielectric and higher leakage current of the MOS device. MOS device at higher temperature is of great importance and relevance at this juncture. In this paper, Al/HfO_2/SiO_2/Si MOS structure is simulated using the Synopsys Sentaurus TCAD simulator and the dependency of the C-V characteristics at higher substrate temperature is studied. It is found here that the accumulation capacitance decreases with the increase of IL thickness due to the reduction of the series capacitance at the IL. The smears of the CV curves confirm the existence of interface trap charges. The high based MOS device with interfacial layer of a thickness of 1 *nm* shows better device performance at higher temperature but its performance deteriorates both for higher IL thickness and without any IL. Therefore, for any application of HfO_2-based MOS device at higher temperature, the IL thickness is of about 1 *nm* is warranted.
Key Words: Conventional SiO_2, TCAD, Gate, MOS, temperature, Curves.

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INTRODUCTION

The progressive down-scaling of bulk metal-oxide-semiconductor field effect transistors (MOSFETs) has been the driving force behind the integrated circuit (IC) industry for several decades, continuously delivering higher component densities and greater chip functionality, while reducing the cost per function from one MOS technology generation to the next. Moore's law boosts IC industry profits by constantly releasing high-quality and inexpensive electronic applications into the market using new technologies. From the 1 µm gate lengths of the eighties to the 35 nm gate lengths of contemporary 45 nm technology, the industry successfully achieved its scaling goals, not only miniaturizing devices but also improving device performance. However, the years of 'happy scaling' are over. Several challenges are facing the further miniaturization of the transistors in Si chips. First, there are the process challenges of continued scaling including, among others, sub-wavelength patterning and the formation of ultra-shallow junctions. Continual process innovation is needed, including immersion optical lithography, and the flash lamp and laser annealing implemented at the 45 nm MOS technology to achieve highfidelity patterns and high-activation/low do pant diffusion. Secondly, the scaling of contemporary deep-decananometer gate length transistors results in the deterioration of electrical characteristics due to short-channel, quantum mechanical and transport effects. Countermeasures like halo-doping can suppress the short-channel effect in conventional MOSFETs but at the expense of increased quantum effects and reduced mobility. Novel MOSFET structures such as fully-depleted silicon-on-insulator devices are required to achieve a fundamental improvement in electrostatic integrity. Finally, intrinsic parameter fluctuations, resulting from the discreteness of charge and the granular nature of matter in real decanano devices, hamper the integration of scaled transistors. Statistical variability unavoidably increases drastically The rapid progress of metal-oxide-semiconductor (MOS) integrated circuit technology has been accomplished by a calculated reduction of the dimensions of the unit device in the

circuit—a practice termed "scaling[1]". Continued device scaling for future technology nodes requires reduction in equivalent oxide thickness (EOT) of gate dielectrics. Extendibility of the conventional Al/HfO2/SiO2/Si gate structure is challenged due to exponential increase in gate leakage currents[2]. A typical HKMG stack structure contains a silicon oxide based interfacial layer (IL), a high-k dielectric, followed by a metal gate electrode. This system is equivalent to two capacitors connected in series. Thus, the total EOT of the HKMG stack can be expressed as follows.

$EOT = EOT_{IL} + EOT_{HK}$ [1]

where EOTIL and EOTHK are contributions from the IL and high-κ layer, respectively. An apparent way to scale EOTHK is to reduce the physical thickness of the high-κ layer, however, there is little room in this direction. It has been reported that a thick HfO2 layer causes significant degradations in carrier mobility and charge trapping both with gate-first[3] and gatelast[4] processes. Therefore, the first generation HKMG devices already employ the thinnest possible high-κ layer. This leaves us with three possible EOT scaling approaches:[12] Introduce a new high-κ material with k-value greater than that of HfO_2;[13] Increase the k-value of IL;[14] Reduce the physical thickness of IL. In this paper, we review current status and challenges for each approach and discuss the EOT scaling strategy for future MOS devices.

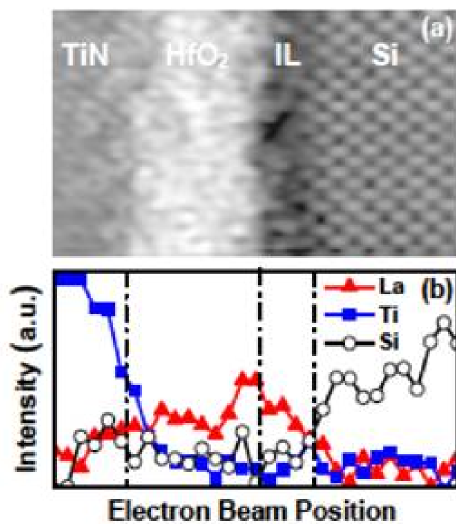

Figure 1: (a) Z-contrast image and (b) corresponding Electron Energy-Loss Spectroscopy (EELS) profiles (La, Ti, and Si) of the SiO2/HfO2/La2O3/TiN/poly-Si stack after a 1,000 °C anneal (after [19]).

HfO_2 is one of the most widely used high-κ materials, showing a k-value of approximately 20. Replacing HfO2 with materials having k-values greater than 20 (higher-κ) is a long term scaling solution. In pursuit of higher-k materials, the tradeoff between k-value and band gap needs to be taken into account. It is generally known that band gap values have a roughly inverse dependence on k-values (Eg~k−0.65)[8]. Therefore, materials with too high k-values typically result in excessive direct tunneling currents and most work showing promising EOT-leakage current density (Jg) characteristics has been achieved with k-value ranging from 20 to 30. Various groups have reported k-value increase in this range by stabilizing the higher-k phase (tetragonal or cubic) of HfO2 via doping of elements such as zirconium[9], yttrium[10], and silicon[11]. This is a practical means to attain a modest k-value increase, however, controllability of crystallinity in an ultra thin HfO2 thickness regime (<2 nm) has yet to be demonstrated. Other groups have suggested La-based higher-k materials such as La-Al-O or La-Lu-O[12]. These materials have recently demonstrated a lot of promise to outperform Hf based.

igh- κ on a device level [13–16].

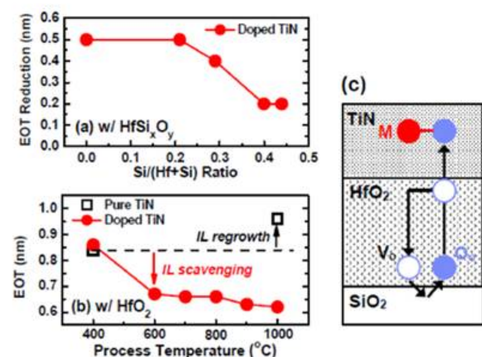

Figure 2: (a)EOT reduction via remoe-scavenging from doped tiN electrodes as a function of Si/(Hf+Si) ratio in HfSixOy gate dielectrics. The EOT reduction is calculated from the difference between the doped TiN and the pure TiN; (b) EOT as a function of maximum process temperature for doped TiN and pure TiN using HfO2 gate dielectrics (after [34]); (c) Schematics of remote scavenging reaction. M, V0, and O0 represent the scavenging element, the oxygen vacancy in HfO2, and the oxygen atom in the lattice position of HfO2, respectively.

The replacement of SiO_2 by a high-k dielectric stack must satisfy a series of material constraints and process integration conditions. Although there are many potential high-k materials, based on their permittivity, a strict selection rules out many candidates. First of all, from a gate leakage perspective, a suitable conduction band offset is necessary to provide a sufficient barrier. For example, tantalum oxide has an adequately high permittivity of around 25, but the ~0.36eV conduction band barrier is not sufficient to provide any overall advantage over SiO_2. The narrower band gap of high-k materials cancels the benefit of the high dielectric constant. Thereby, a suitable trade-off between the

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dielectric constant and the conduction band offset is the first criterion for high-k dielectric candidates[15]. A few high-k dielectrics show the promise to replace silicon oxide, and some of their fundamental parameters are listed in Table 1 along with the corresponding parameters of SiO_2 [15,16,17].

Table 1: Some essential parameters for selected high-k materials and SiO_2

Material	Band gap	Relative dielectric constant	Conduction band offset (eV)	Leakage current reduction (ref SiO_2)	Thermal stability T_{max} (^{0}C)
SiO_2	9	3.9	3.15	-	-
Si	4	1.2	1.25	-	-
Al2O3	8.8	9.5-12	2.8	10^2-10^3	~1000
HfO_2	4.5-6	16-30	1.5	10^4-10^5	~430-600
$HfSiO_4$	~6	~10	1.5		

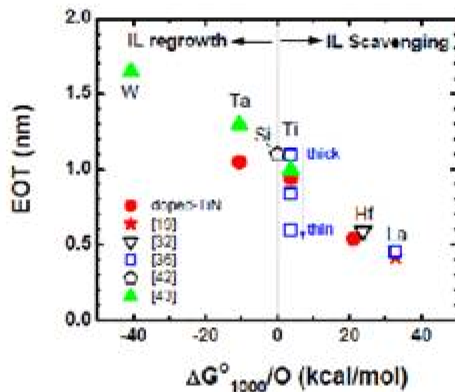

Figure 3: EOT of SiO2/HfO2 metal-inserted poly-Si stack (MIPS) structure as a function of ΔG0 1000 per oxygen atom for scavenging element. TiN electrodes doped with various metals are compared with literature data (after[19,32,36,42,43]). The ΔG0 1000 values are after[41].

CONCLUSION

The effect of rapid thermal annealing on the oxide charge distribution of Al/HfO2/SiO2/Si metal---oxide---semiconductor structures are studied using technology computer-aided design (TCAD) simulations and experiments. The simulated electrical characteristics are compared with experimentally obtained data. The interface traps are found to be nonuniform in nature and laterally distributed following a Gaussian profile. The distribution of interface trap charges arises because of spatial electric field variation in the oxide film upon gate bias application. The interface trap density is found to decrease with increase in annealing temperature. It is further observed that, at higher annealing temperature, the fixed oxide charge density increases due to interfacial Hf silicate formation.

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